

FIG. 1

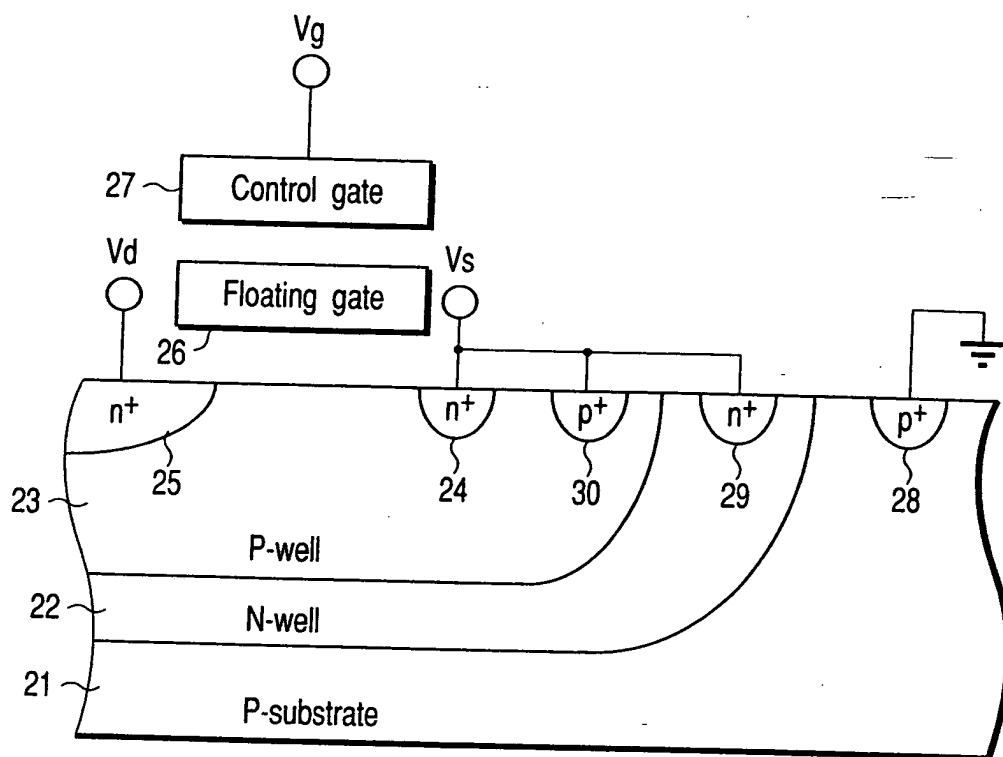


FIG. 2A

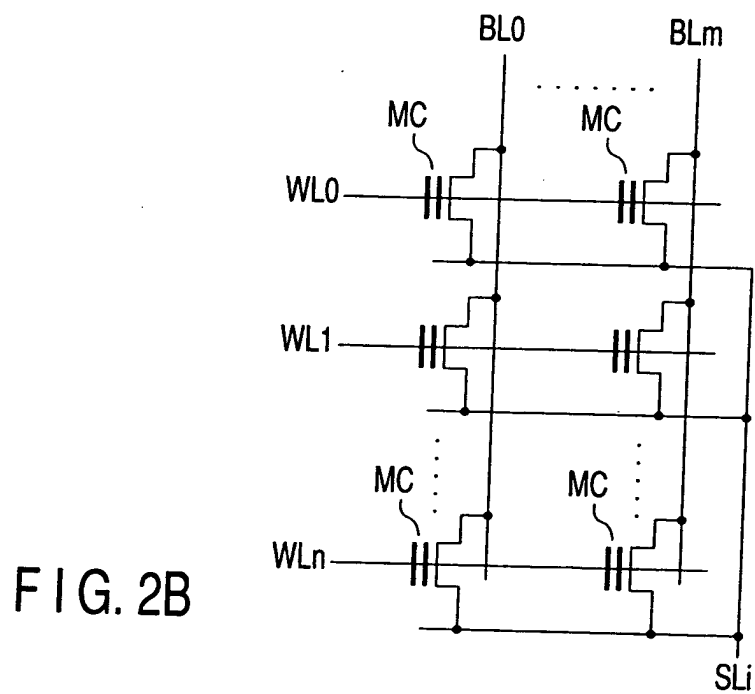


FIG. 2B

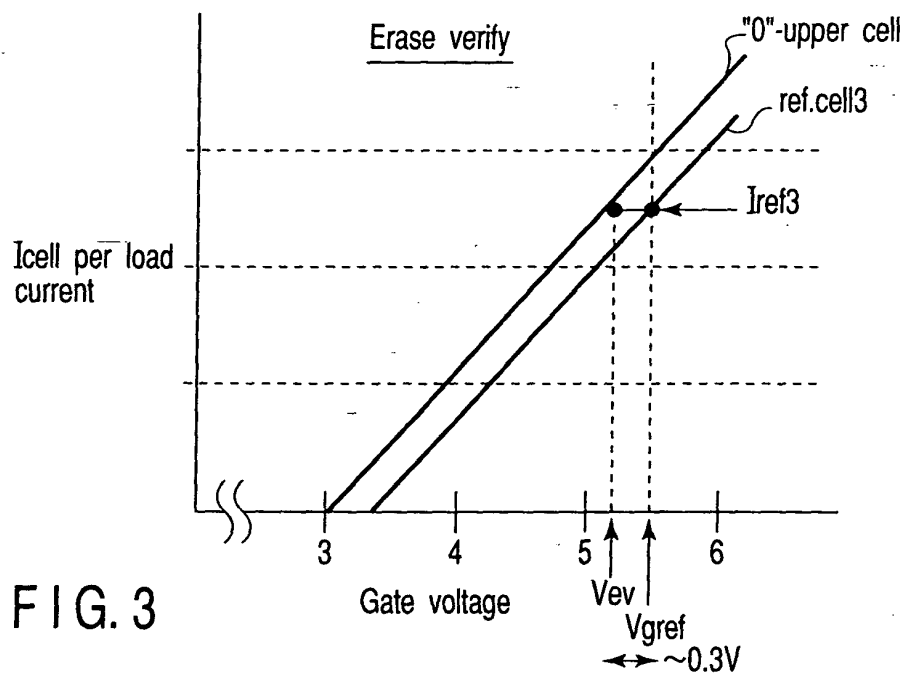


FIG. 3

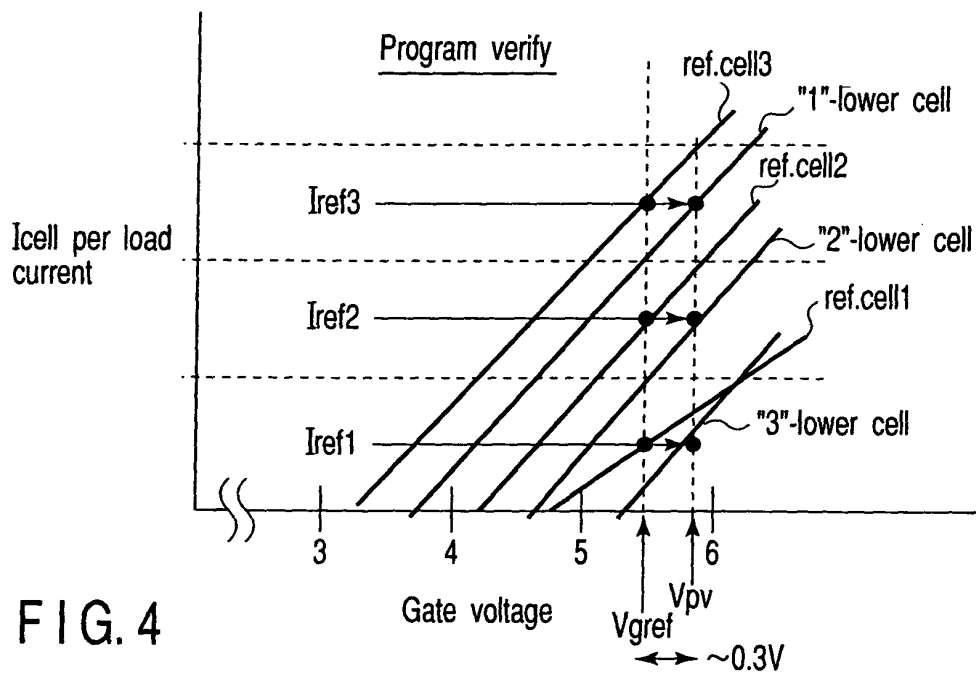
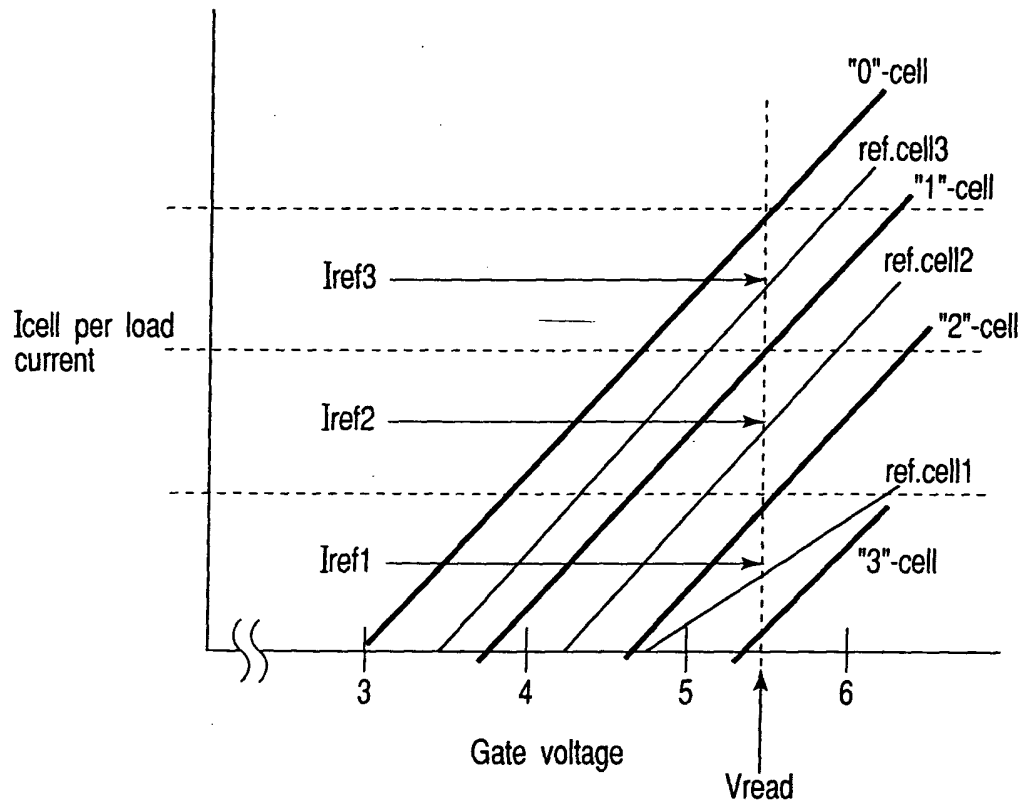


FIG. 4

Distribution of 4-level and read

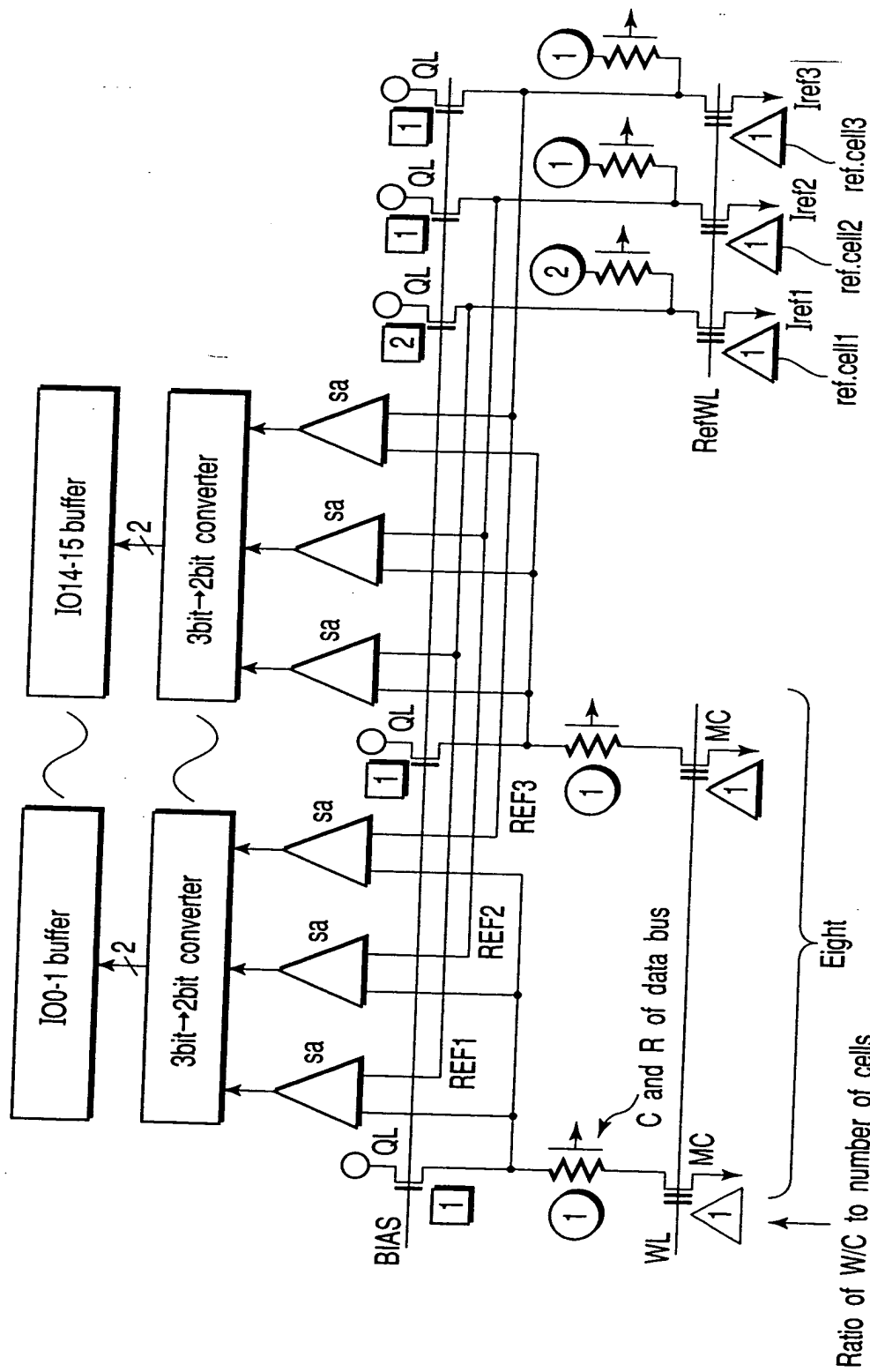


During read : $V_g = V_{ddr}$ (memory cell, reference cell)

During verify : $V_g = V_{sw}$ (memory cell)

$V_g = V_{swref}$ (reference cell)

FIG. 5



Ratio of W/C to number of cells

Eight

FIG. 6

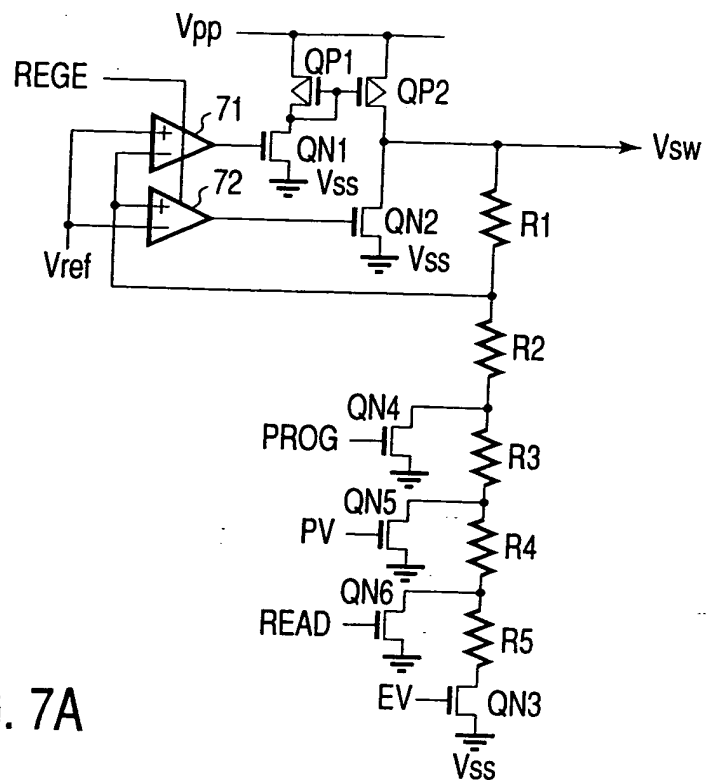


FIG. 7A

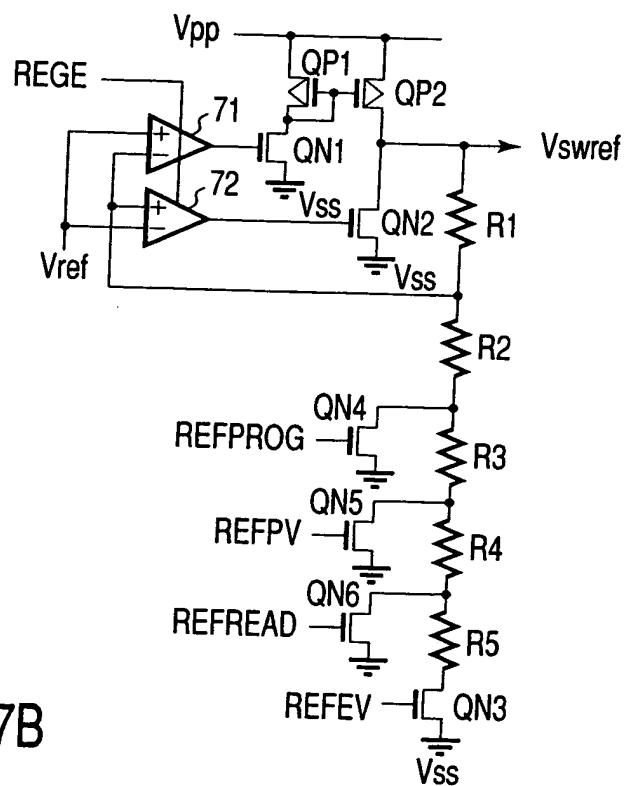
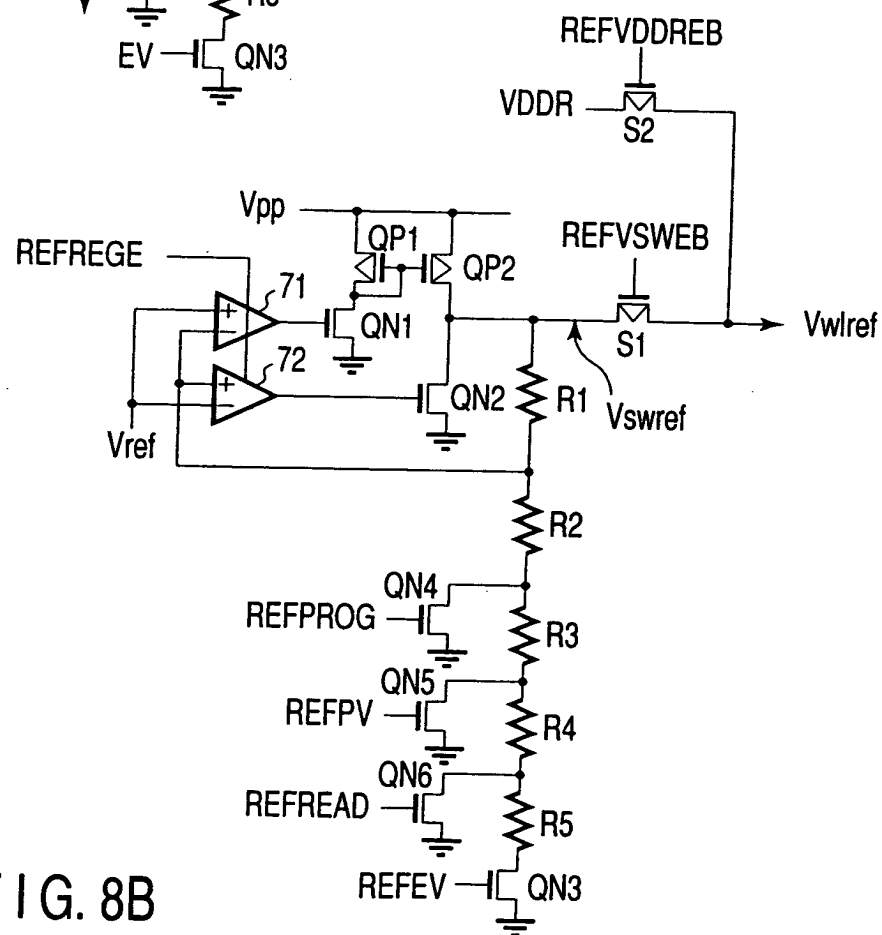
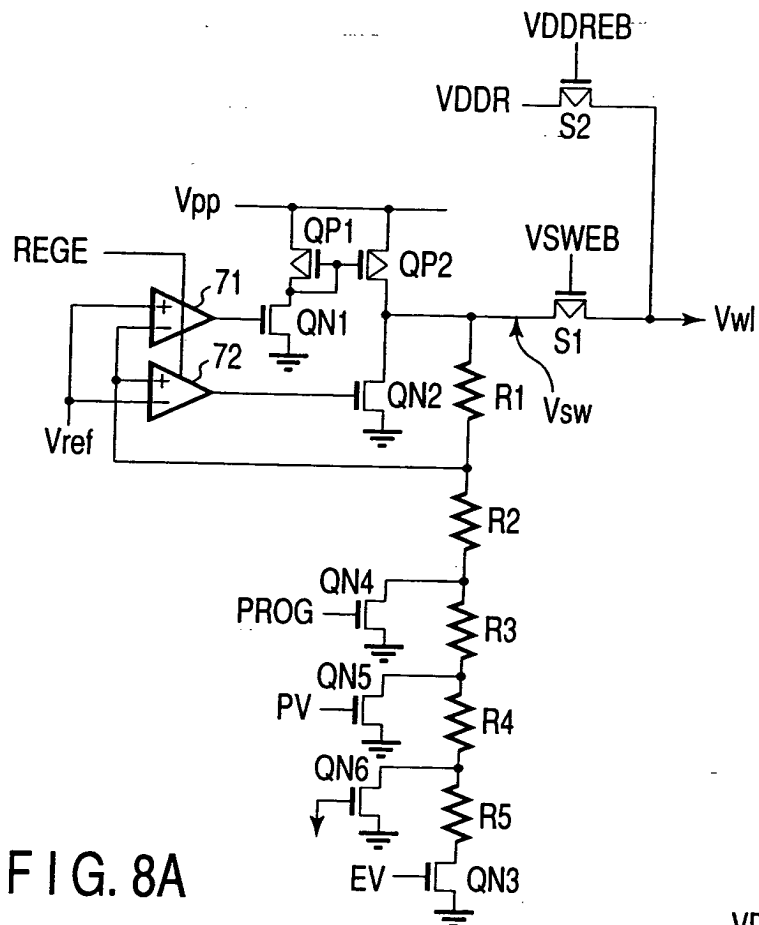


FIG. 7B



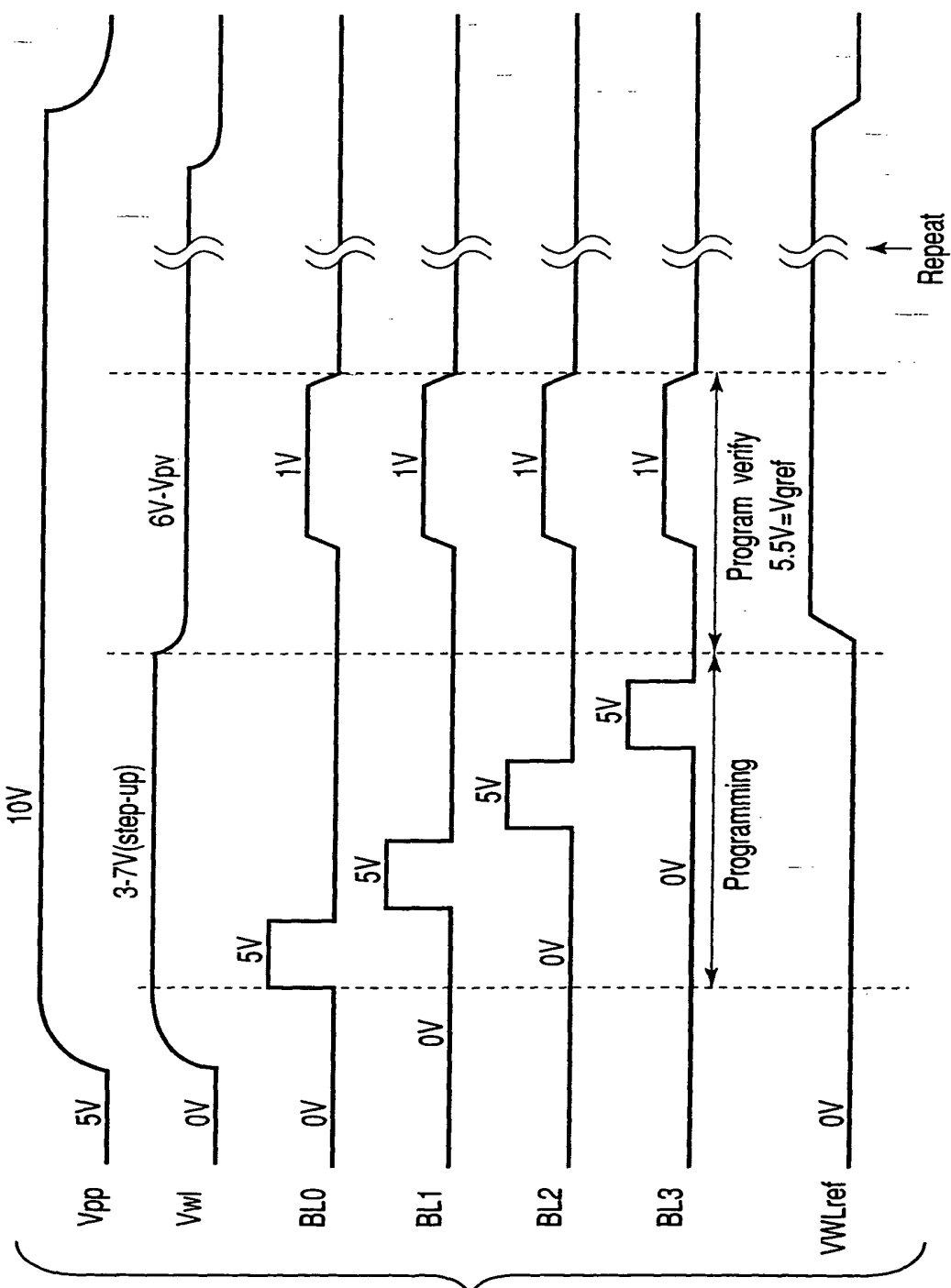


FIG. 9

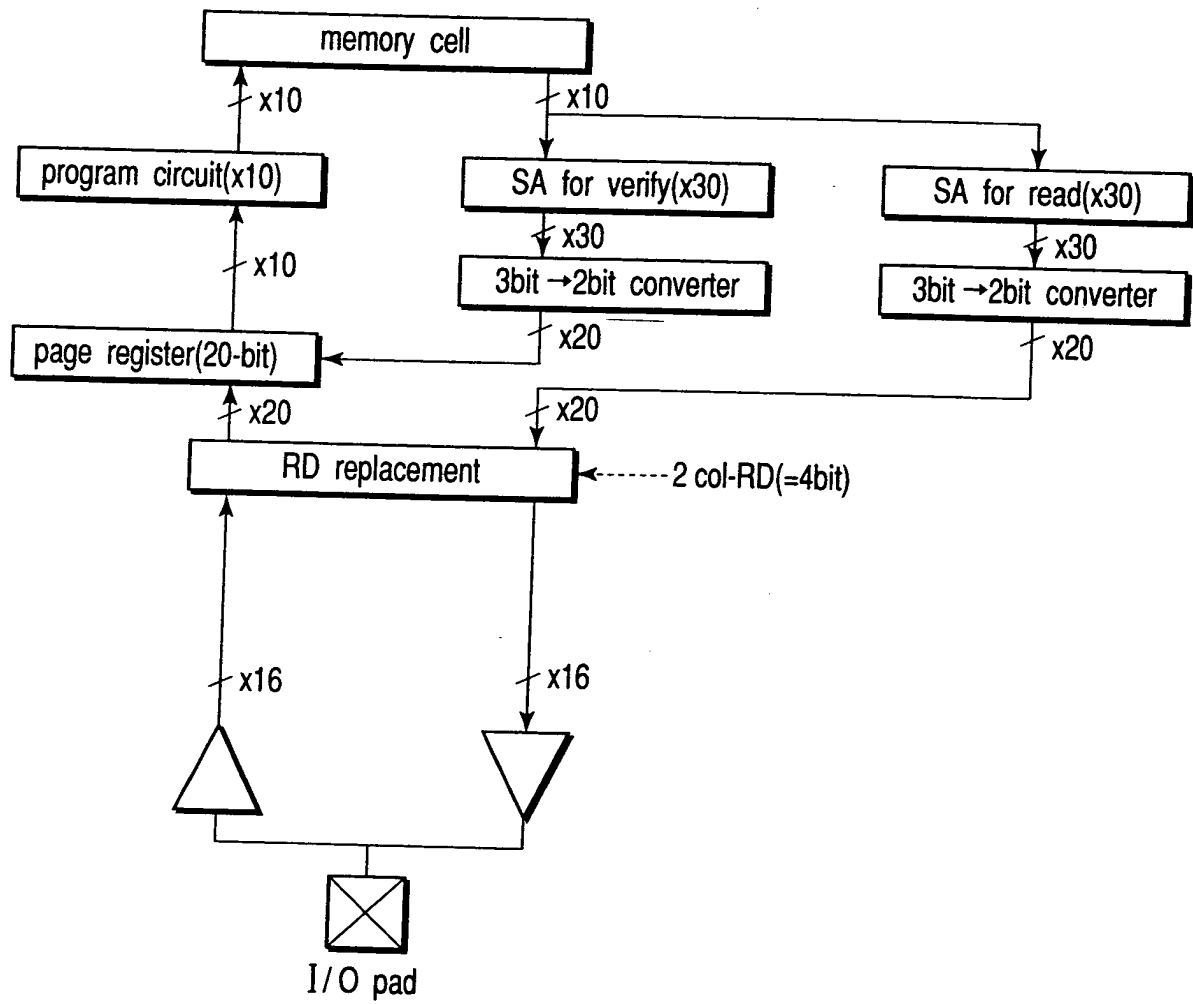


FIG. 10

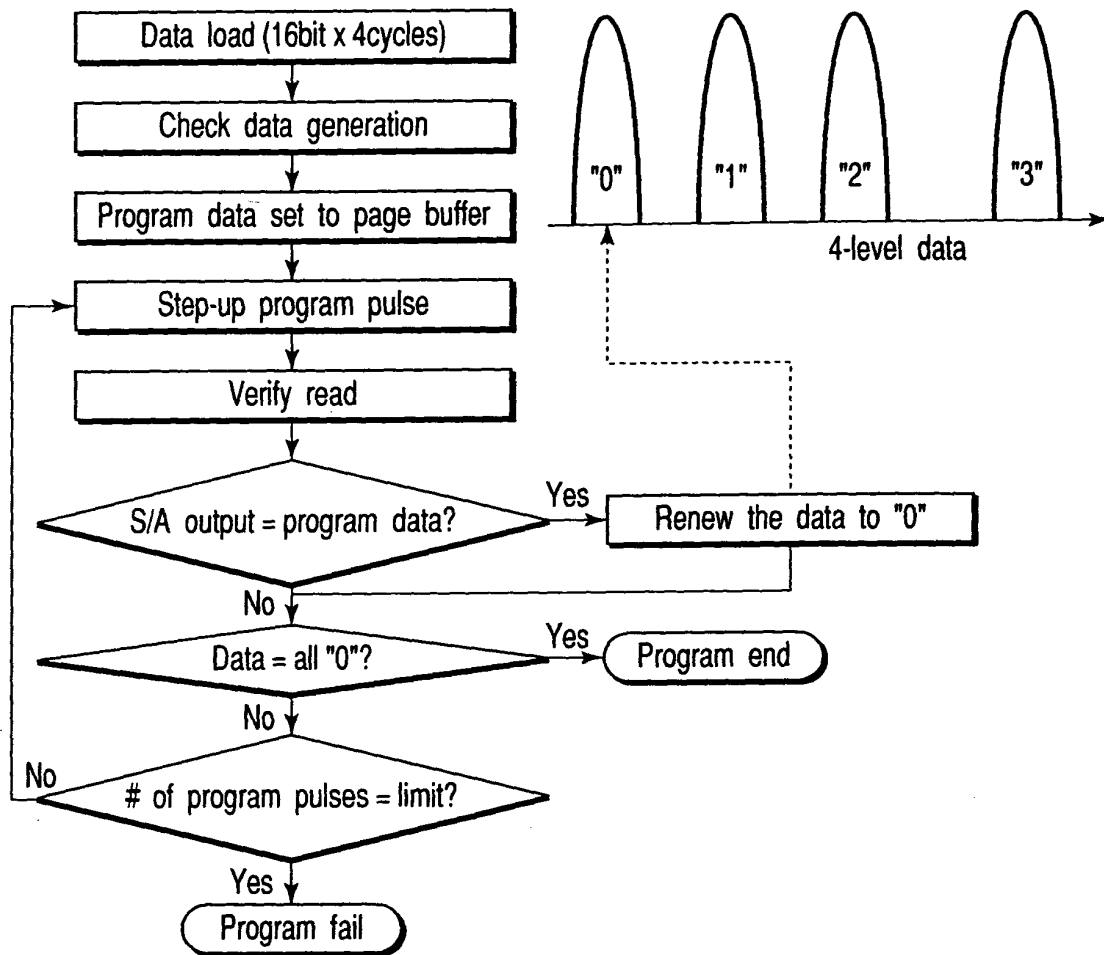


FIG. 11

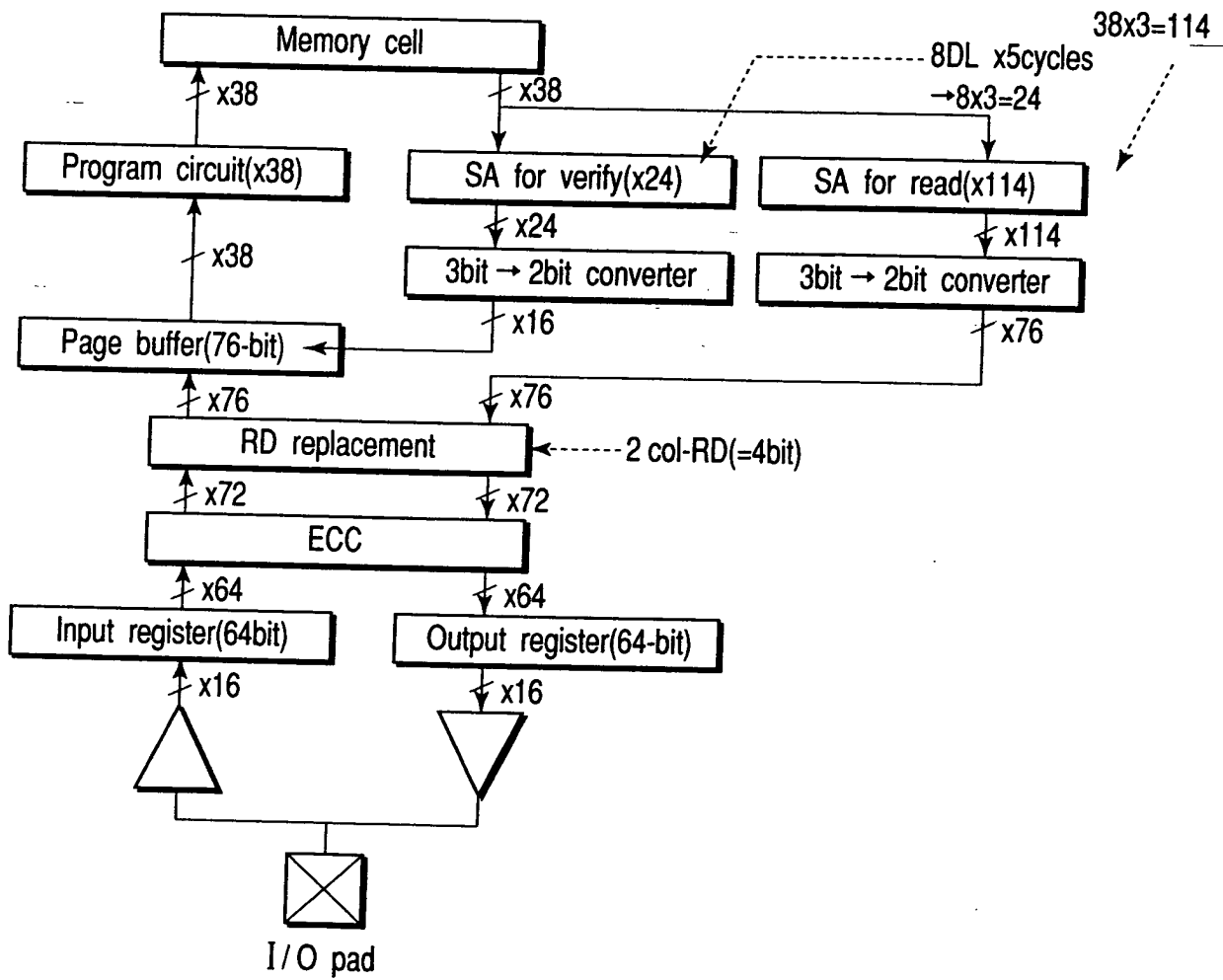
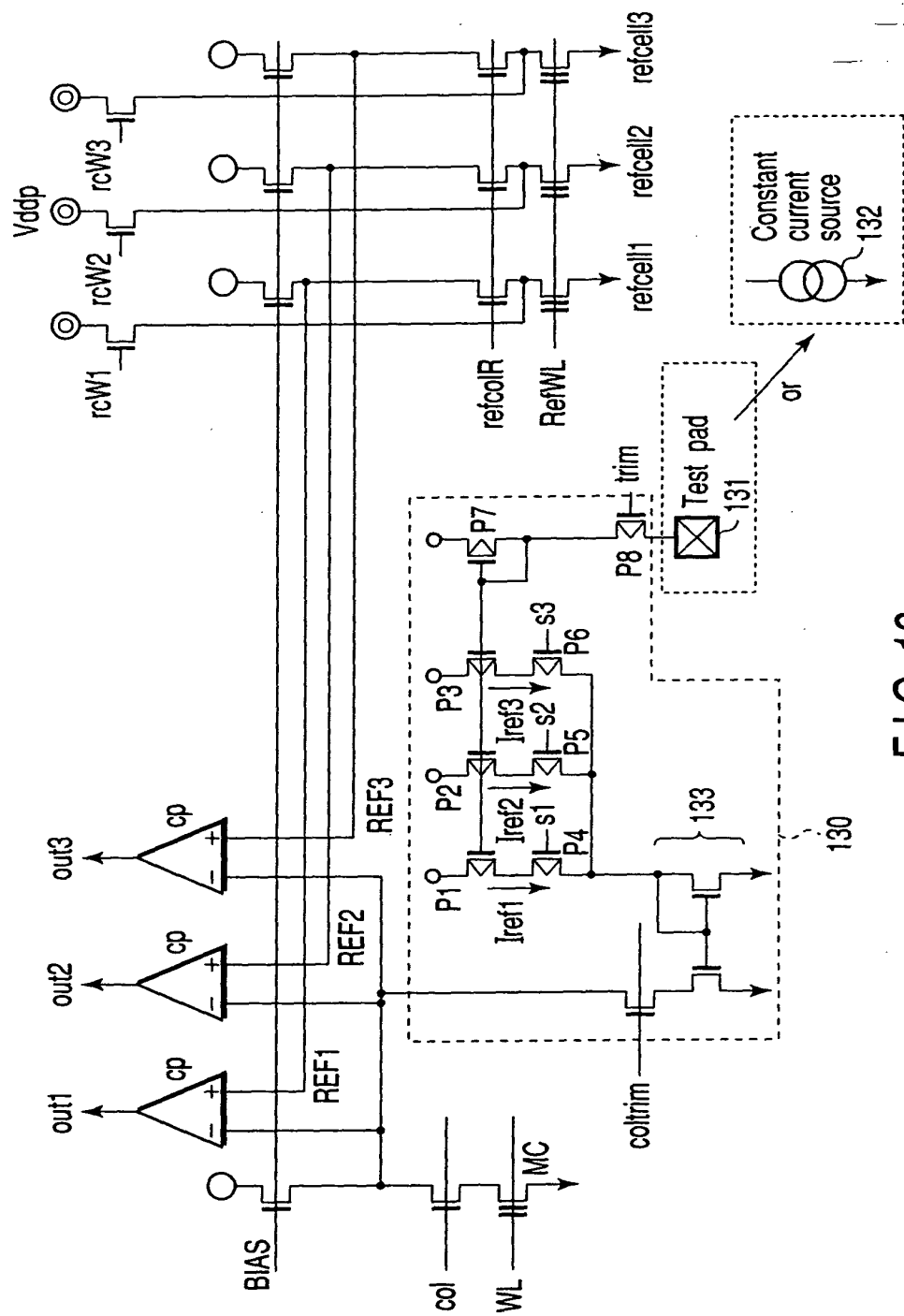


FIG. 12



WL=0v
 Col=0v
 Coltrim=5v
 Trim=0v
 Vddp=5v

	s1	s2	s3	refWL	refcolR	rcw1	rcw2	rcw3	out1	out2	out3
Step1	Erase reference cells										
Step2	0v	5v	5v	5v	5v	0v	0v	0v	out1:L→step3/H→step4		
Step3	0v	5v	5v	9v	0v	9v	0v	0v	→step2		
Step4	5v	0v	5v	5v	5v	0v	0v	0v	out2:L→step5/H→step6		
Step5	5v	0v	5v	9v	0v	0v	9v	0v	→step4		
Step6	5v	5v	0v	5v	5v	0v	0v	0v	out3:L→step7/H→step8		
Step7	5v	5v	0v	9v	0v	0v	0v	9v	→step8		
Step8	Trim end										

FIG. 14

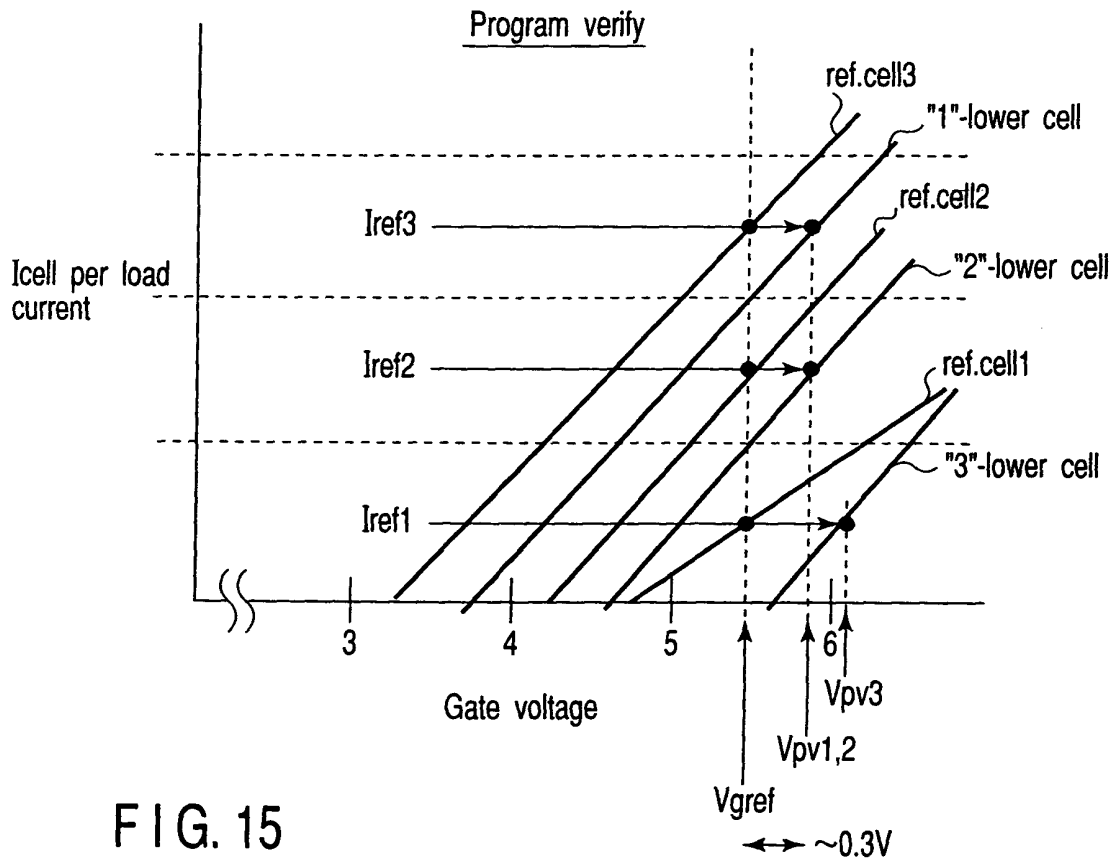
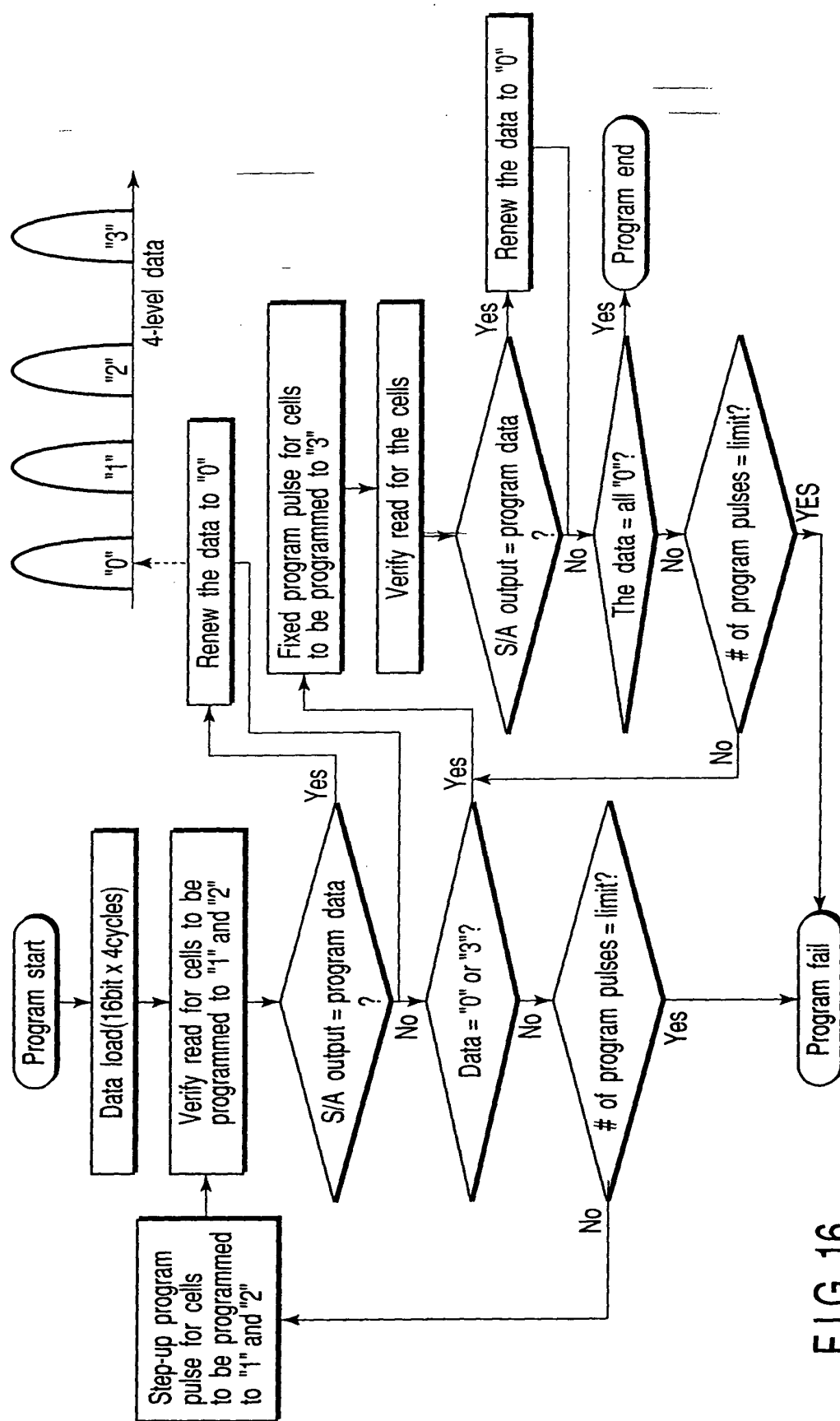


FIG. 15



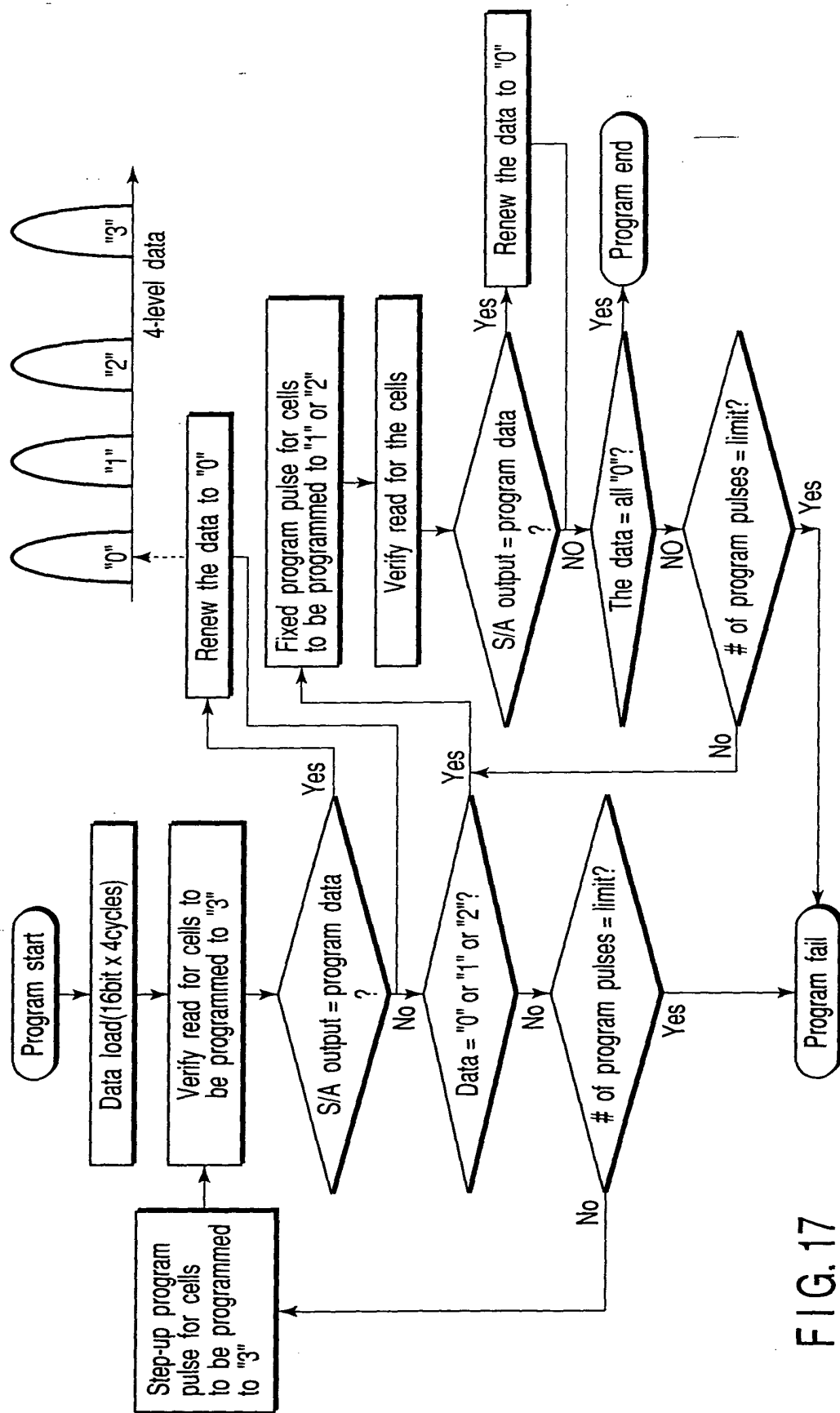


FIG. 17

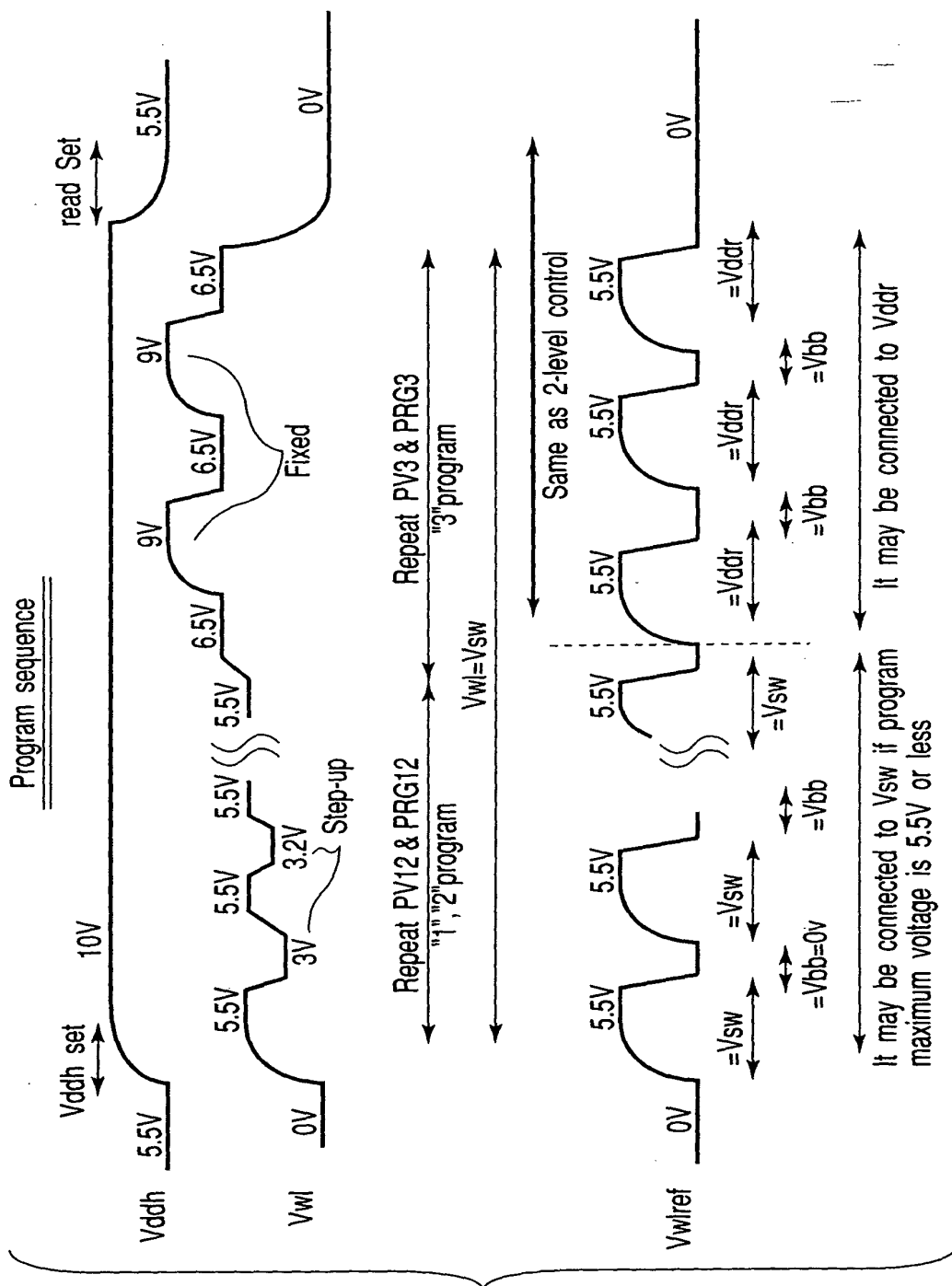


FIG. 19

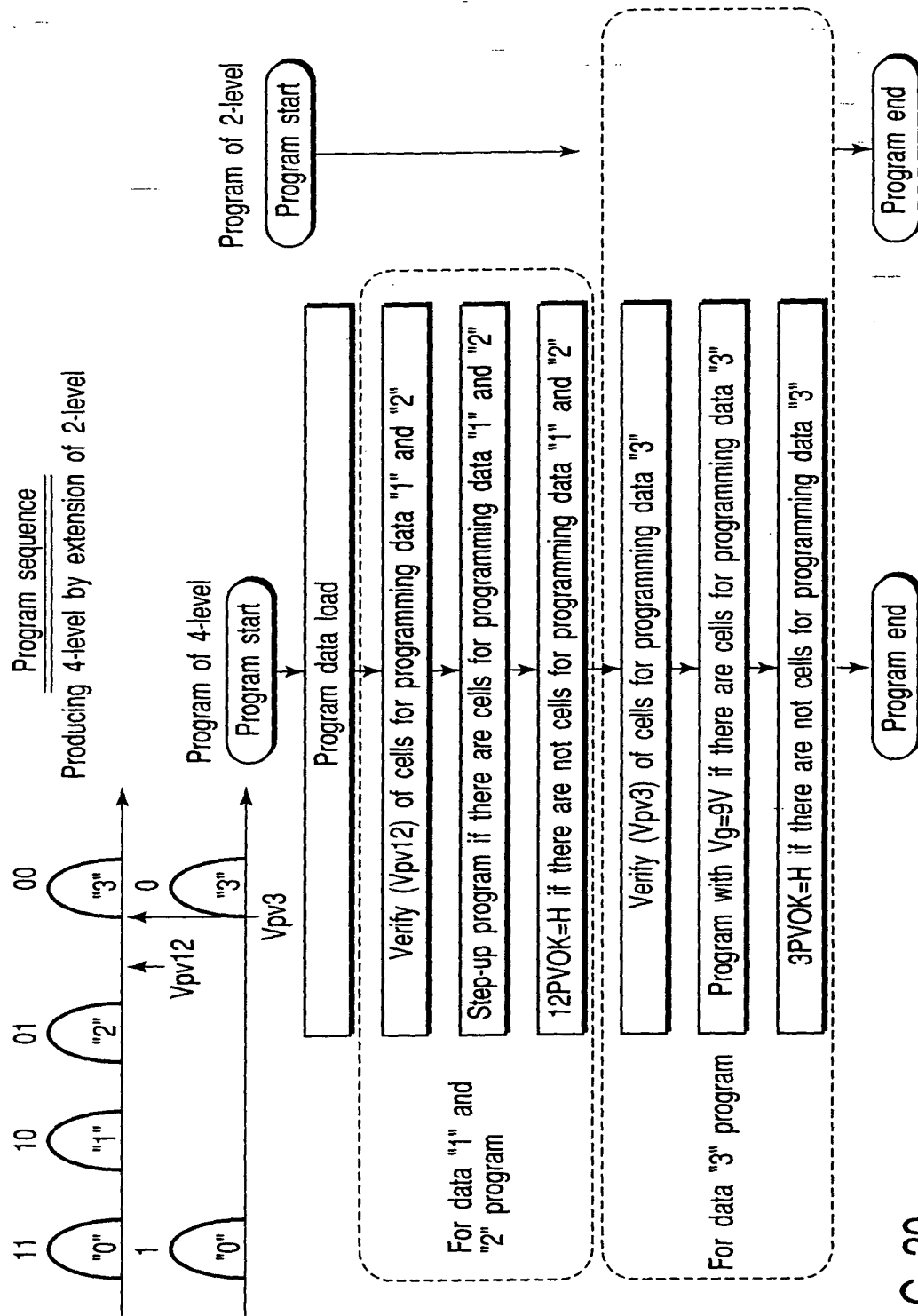


FIG. 20

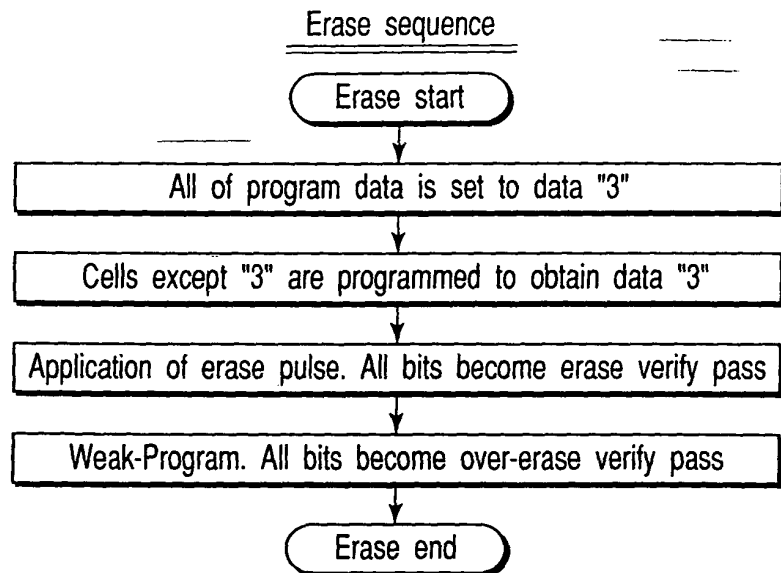


FIG. 21

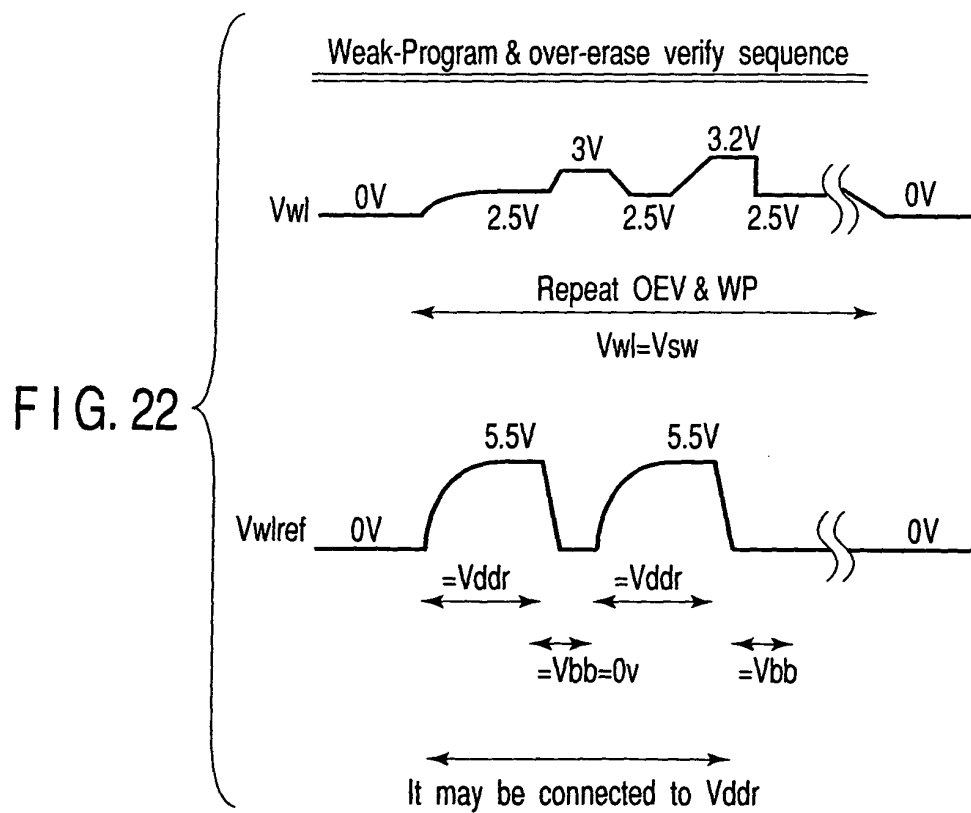


FIG. 22

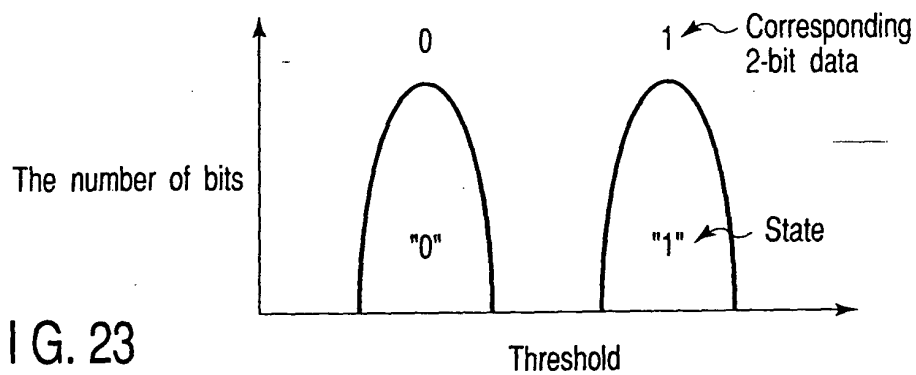


FIG. 23
(Prior art)

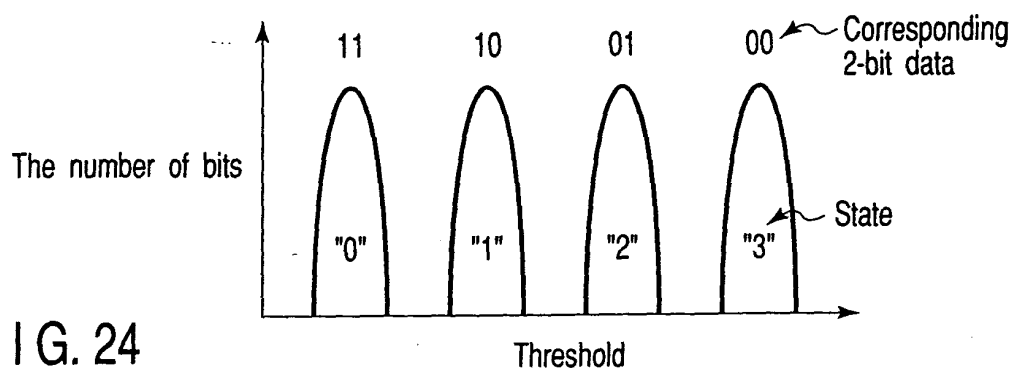


FIG. 24
(Prior art)

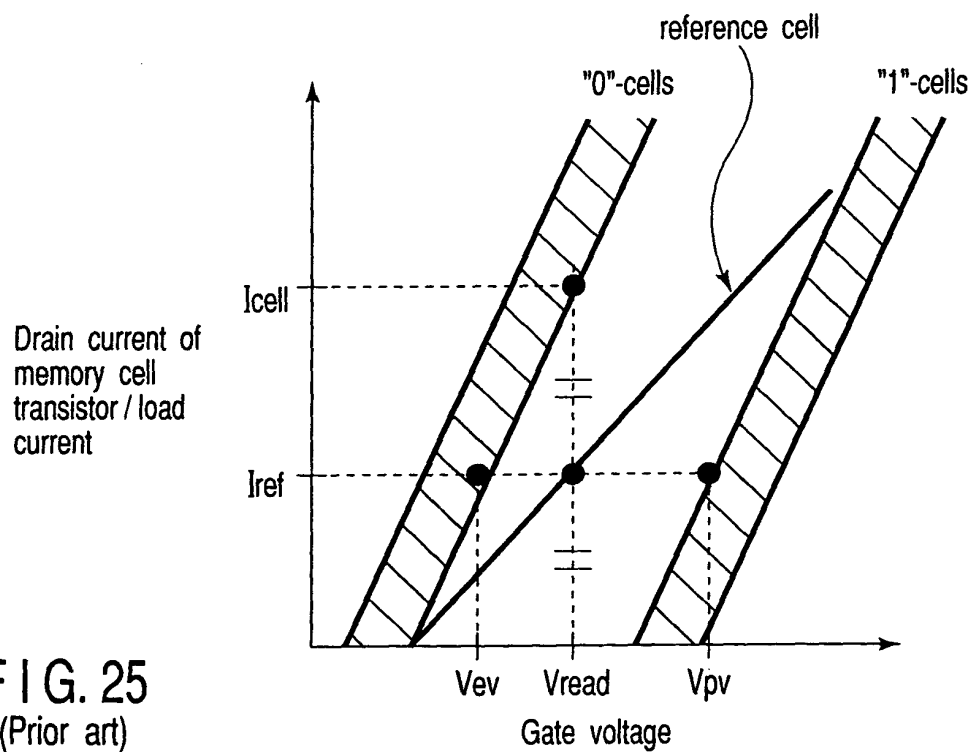


FIG. 25
(Prior art)

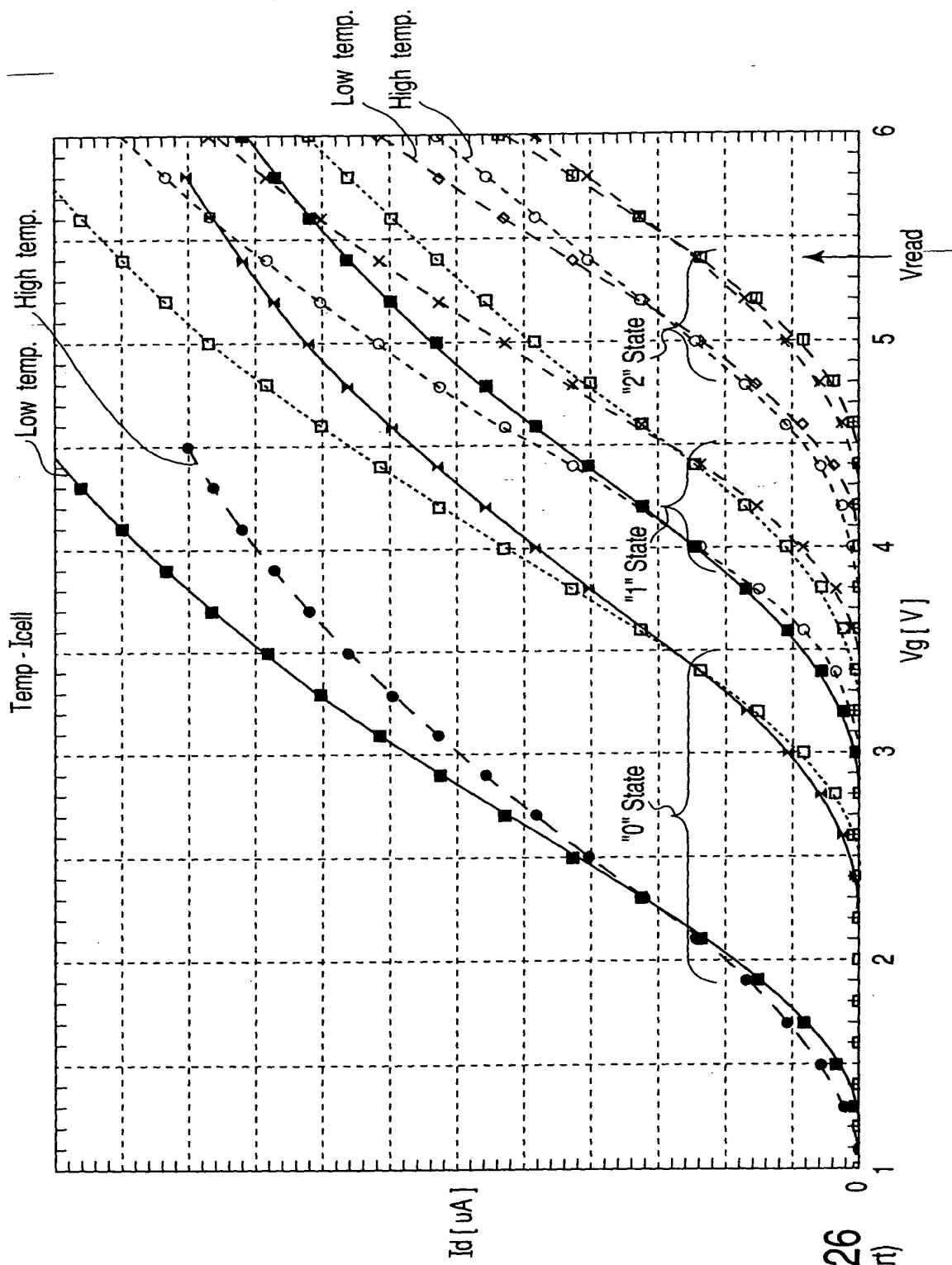


FIG. 26
(Prior art)